09/377182

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,584,482 B1
DATED : June 24, 2003
INVENTOR(S) : Craig C. Hansen et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page showing the illustrative figure should be deleted to be replaced with the attached title page.

Drawing sheet, consisting of Figs. 5A-5B, should be deleted to be replaced with the drawing sheet, consisting of Figs. 5A-5B, as shown on the attached page.

Signed and Sealed this

Twelfth Day of April, 2005

JON W. DUDAS
Director of the United States Patent and Trademark Office

09/377,182

(12) **United States Patent**
Hansen et al.

(10) **Patent No.: US 6,584,482 B1**
(45) **Date of Patent: *Jun. 24, 2003**

(54) **MULTIPLIER ARRAY PROCESSING SYSTEM WITH ENHANCED UTILIZATION AT LOWER PRECISION**

(75) Inventors: **Craig C. Hansen**, Los Altos, CA (US); **Henry Massalin**, Sunnyvale, CA (US)

(73) Assignee: **Microunity Systems Engineering, Inc.**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **09/377,182**

(22) Filed: **Aug. 19, 1999**

Related U.S. Application Data

(63) Continuation of application No. 08/857,596, filed on May 16, 1997, now Pat. No. 5,953,241, which is a continuation-in-part of application No. 08/516,036, filed on Aug. 16, 1995, now Pat. No. 5,742,840.
(60) Provisional application No. 60/021,132, filed on May 17, 1996.

(51) **Int. Cl.**[7] **G06F 17/15**

(52) **U.S. Cl.** **708/523**; 708/420; 708/501; 708/603; 712/221

(58) **Field of Search** 708/523, 501, 708/319, 603, 420; 712/221

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,876,660	A	10/1989	Owen et al.	364/764
4,956,801	A	9/1990	Prem et al.	364/748
4,969,118	A	11/1990	Montoye et al.	364/748
5,032,865	A	7/1991	Schlunt	364/750.5
5,408,581	A	4/1995	Suzuki et al.	364/724.16
5,500,811	A	3/1996	Corry	364/724.16

Primary Examiner—David H. Malzahn
(74) *Attorney, Agent, or Firm*—McDermott, Will & Emery

(57) **ABSTRACT**

A multiplier array processing system which improves the utilization of the multiplier and adder array for lower-precision arithmetic is described. New instructions are defined which provide for the deployment of additional multiply and add operations as a result of a single instruction, and for the deployment of greater multiply and add operands as the symbol size is decreased.

23 Claims, 13 Drawing Sheets

Group Fixed-point Multiply and Sum

- Group Multiply and Sum: 64/128 bits := 128*128 bits
  - symbol sizes of 1, 2, 4, 8, 16, 32, 64 bits

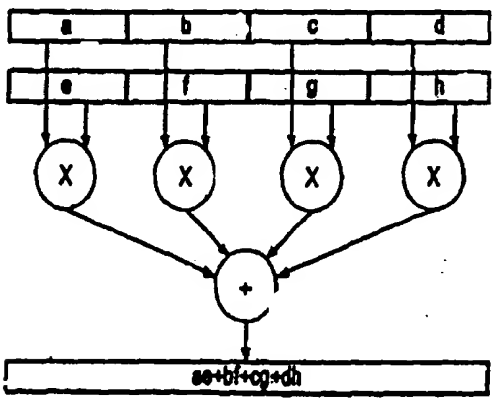


Figure 5A

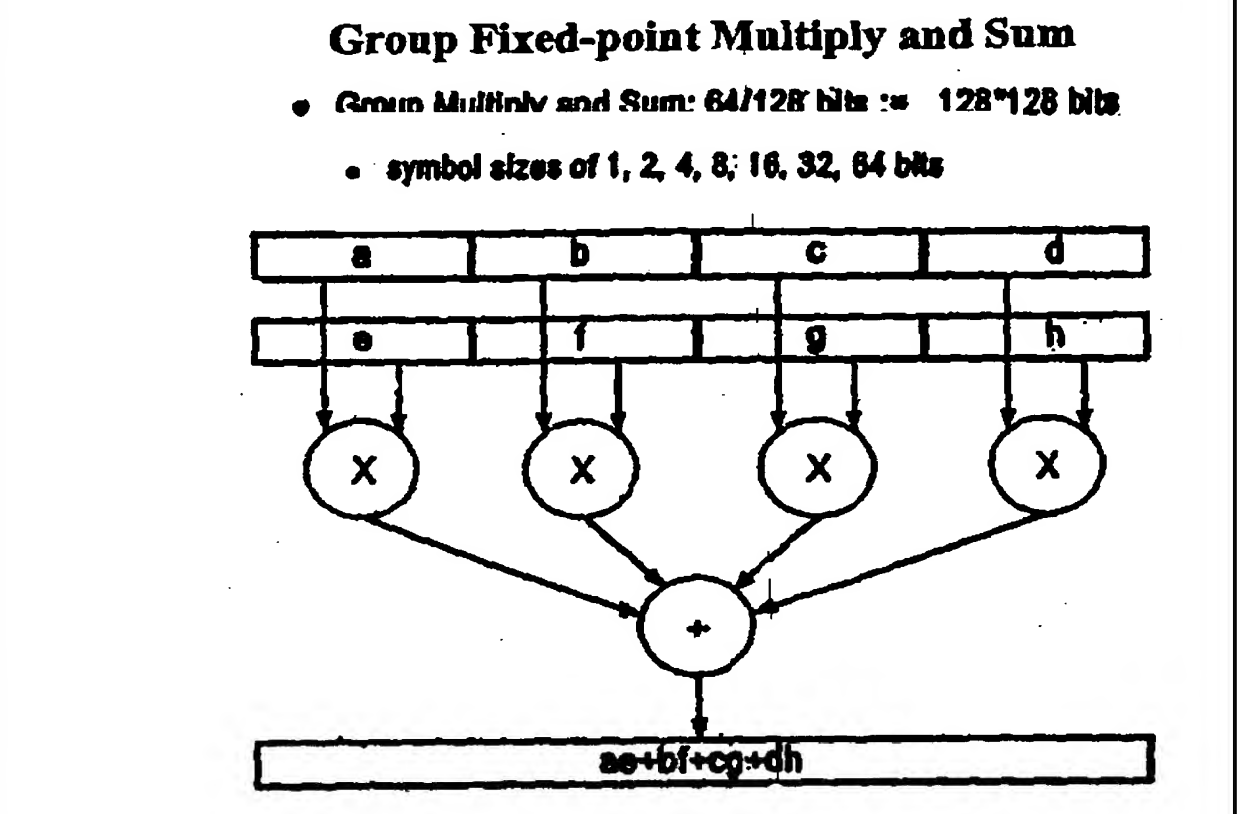
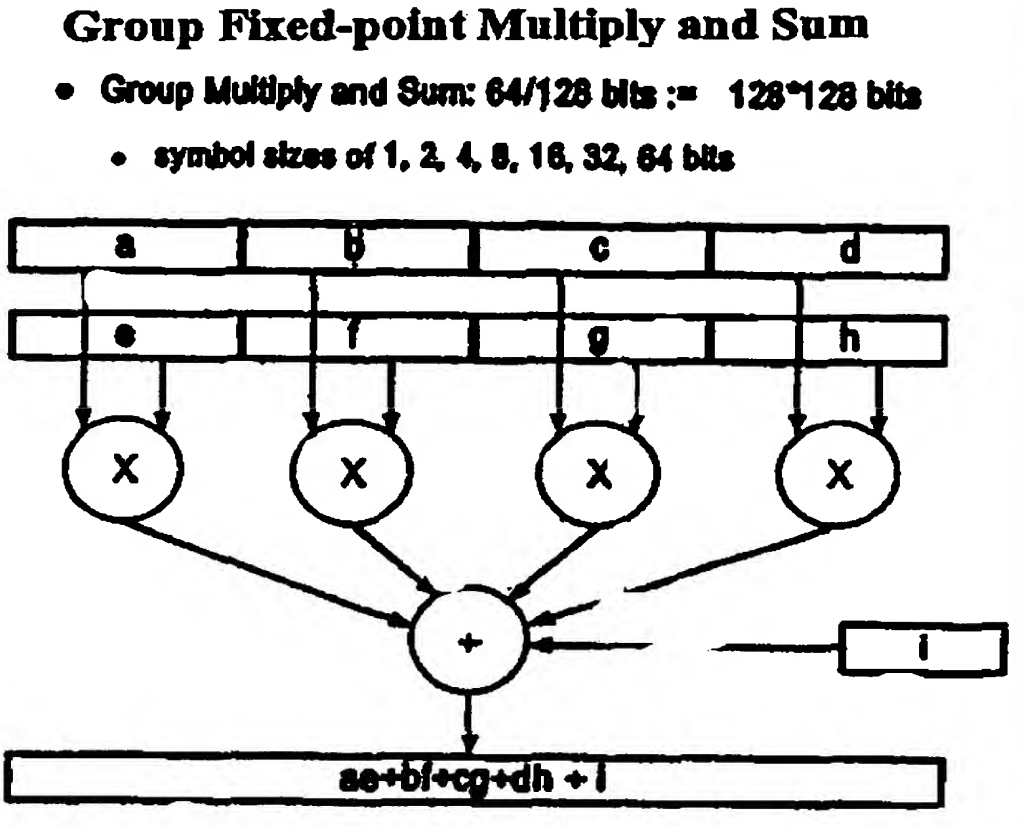


Figure 5B


Group Fixed-point Multiply and Sum
• Group Multiply and Sum: 64/128 bits := 128*128 bits
• symbol sizes of 1, 2, 4, 8, 16, 32, 64 bits
a
b
c
d
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f
g
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ae+bf+cg+dh + i